CLAIMS

What is claimed is:

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1. A system for transferring data between a plurality of devices communicably coupled to a bus, the bus including at least one data line for transmitting the data and at least one clock line, the system comprising:

the system being operative at a first clock rate and at a second clock rate less than the first clock rate;

a first device communicably coupled to the bus and operative at least at the second clock rate to store at least a portion of the data in a register; and

a second device communicably coupled to the bus and operative at least at the second clock rate to drive the clock line to a low logic level while the data is stored in the register of the first device.

2. The system of claim 1 wherein the first device is further operative at least at the second clock rate to clear the data from the register upon completion of a data transfer.

3. The system of claim 1 further including pull-up circuitry for pulling the clock line to a high logic level, and wherein the second device is further operative to release the clock line upon completion of a data transfer to allow the clock line to be pulled-high by the pull-up circuitry.

4. The system of claim 1 further including pull-up circuitry for pulling the clock line to a high logic level,

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and wherein, upon completion of a data transfer, the first device is further operative to clear the data from the register and the second device is further operative to release the clock line to allow the clock line to be pulled-high by the pull-up circuitry.

5. The system of claim 1 wherein the bus comprises an SMBus.

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6. A method for transferring data between a plurality of devices communicably coupled to a bus, the bus including at least one data line for transmitting the data and at least one clock line for transmitting a clock signal at a first clock rate and at a second clock rate less than the first clock rate, the method comprising the steps of:

while the clock signal is being transmitted at least at the second clock rate, storing at least a portion of the data in a register communicably coupled to the bus; and

driving the clock line to a low logic level while the data is stored in the register.

7. The method of claim 6 further including the step of clearing the data from the register upon completion of a data transfer.

8. The method of claim 6 wherein the clock line is pulled to a high logic level by pull-up circuitry, and further including the step of releasing the clock line upon completion of a data transfer to allow the clock line to be pulled-high by the pull-up circuitry.

9. The method of claim 6 wherein the clock line is pulled to a high logic level by pull-up circuitry, and further including the steps of, upon completion of a data transfer, clearing the data from the register and releasing the clock line to allow the clock line to be pulled-high by the pull-up circuitry.